

CHORUS 4 CHIP

APPLICATIONS

- Clock radios
- Smart Radios
- Smart Speakers
- Spotify Speakers
- Home audio systems.

OVERVIEW

Chorus 4 is the world's first fully integrated smart radio system-on-chip (SoC). Incorporating RF Tuner, baseband, application processor, audio decode, and DAC functionality and integrated SDRAM. Chorus 4 is a fully integrated single chip radio receiver SoC, performance optimised for Smart Radio and speaker applications, for example, internet radio, Spotify Connect, Bluetooth, DAB/DAB+ and FM-RDS products.

Chorus 4 has been designed to power all major categories of consumer Smart radio Radio devices from low cost smart radios to premium home audio systems. Chorus 4 streams radio and music files in a variety of formats including AAC, AAC+, MP3, WAV, and FLAC. The chip also supports a full colour display.

Containing a number of innovative technologies to optimise system performance, and cost optimised whilst inheriting market leading Smart Radio features. The high level of integration helps to reduce the system component count and complexity associated with integrating an external DAB and application processor. Overall, helping to keep the BoM costs to a minimum as well as reducing manufacturing time and costs.

Chorus 4 is Digital Tick compliant. The on-chip multi-band RF tuner and processor operate in the following RF bands; LW/MW/SW, FM, and DAB-III and DAB-L.

FEATURES

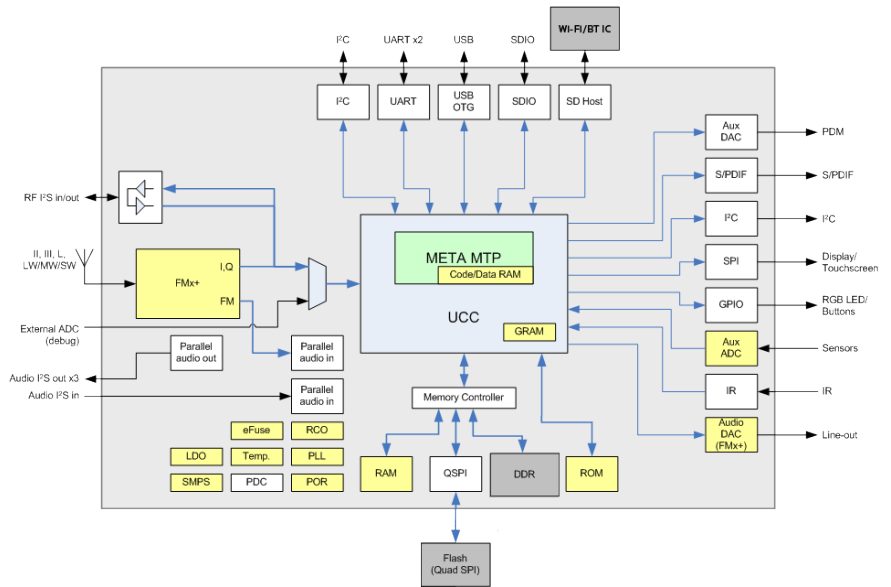
- CPU 360MHz META MTP
- On-chip DDR-RAM
- RF Sensitivity: DAB -100dBm, FM -110dBm
- On board RF tuner supporting Band L, Band III, Band II, Band I, UPC cabled DAB
- Internal Stereo DAC with 90dB dynamic range
- Boot from internal memory, SPI flash memory or host device. Software configurable
- Flash memory interface
- power-on reset circuit
- on-chip voltage regulator
- Temperature range
- Operating 0 to +70 °C
- Storage -40 to +125 °C
- Full RoHS compliance.

CHORUS 4 FS1440

Advanced digital radio and audio baseband network processor

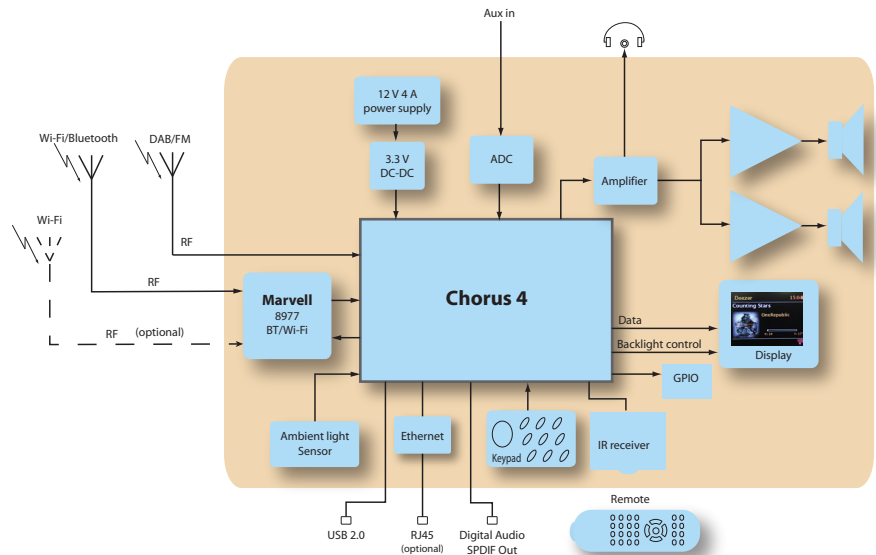
EXTENSIVE INTERFACES

- Multiple configurable GPIO and ADC inputs
- High-speed USB 2.0 for DFU
- S/PDIF audio output
- I2S input/output of decoded audio data (both master and slave modes)
- Support for multiple SPI slave devices
- 2 x 16550-compliant UARTs with optional flow control
- Colour LCD/OLED supported via SPI/I2C or LED indicators for headless display.
- JTAG interface for test and emulator support
- Ethernet interface via SDIOSPI
- Support for Marvell 8977 dual band WIFI/BT combo.



ARCHITECTURE

The META multithreaded core is a high-performance low-power modular device enabling extensive customisation. It is designed for use in applications such as audio signal processing and next-generation digital wireless.



SIMPLE DAB/MP3
PLAYER APPLICATION

Processor architecture	Multithreaded 3-operand register based
Data types and registers	16/32-bit integer ALU with multiple 32-bit register files
System architecture	Independent 64-bit instruction and data interfaces
Exceptions and interrupts	Memory, instruction, and interrupt handling on each thread
Instruction set	RISC 32-bit with 64-bit extensions
Pipeline	3-stage



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